CLAIMS

What is claimed is:

1. A system for saving the state of an integrated circuit, the system comprising:

a non-volatile memory; and

a state-saving controller coupled to the non-volatile memory and coupled to the integrated circuit, wherein the state-saving controller saves the state of the integrated circuit to the non-volatile memory when a failure occurs in the integrated circuit.

2. The system of claim 1 wherein the state-saving controller saves the state of substantially all latches of the integrated circuit to the non-volatile memory when a failure occurs in the integrated circuit.

3. The system of claim 1 wherein the state of each latch is saved when the failure is an unrecoverable error in the integrated circuit.

4. The system of claim 1 wherein the integrated circuit is an Application Specific Integrated Circuit (ASIC).

5. The system of claim 1 wherein the non-volatile memory is an Electrically-Erasable Programmable Read Only Memory (EEPROM).

6. The system of claim 1 wherein the state-saving controller is a separate component

electrically coupled to the integrated circuit and to the non-volatile memory via a bus.

7. The system of claim 6 wherein the state-saving controller is a bus master of the bus.

8. The system of claim 6 wherein the bus is a serial bus.

9. The system of claim 1 wherein the state-saving controller is integrated with and internal to the integrated circuit.

10. The system of claim 1 wherein the non-volatile memory is a separate component electrically coupled to the integrated circuit by a bus.

11. The system of claim 1 wherein the non-volatile memory is integrated with and internal to the integrated circuit.

12. The system of claim 1 further comprising at least one additional integrated circuit, wherein the additional integrated circuit is coupled to the non-volatile memory and to the state-saving controller, and wherein the state-saving controller saves the state of the additional integrated circuit to the non-volatile memory when a failure occurs in the additional integrated circuit.

13. The system of claim 1 wherein the saved state of the integrated circuit includes the data contents of registers and other latches of the integrated circuit.

14. A method for saving the state of an integrated circuit, the method comprising:

determining that an error has occurred in the operation of the integrated circuit; and

saving the state of the integrated circuit to a non-volatile memory coupled to the integrated circuit, the state saved after the error has been detected.

15. The method of claim 14 wherein the states of substantially all latches of the integrated circuit are saved to the non-volatile memory.

16. The method of claim 14 wherein the state is saved when the error is an unrecoverable error in the integrated circuit.

17. The method of claim 14 wherein all internal clocks of the integrated circuit are stopped so that the latches retain their states upon the error in the operation of the integrated circuit.

18. The method of claim 14 wherein an error flag is asserted after the state of the integrated circuit has been saved.

19. The method of claim 18 wherein the error flag is provided to a service processor monitoring the operation of the integrated circuit.

20. The method of claim 14 wherein the state of the integrated circuit is saved by a state-saving controller coupled to the non-volatile memory and coupled to the integrated circuit.

21. The method of claim 14 wherein the integrated circuit is an Application Specific Integrated Circuit (ASIC).

22. The method of claim 14 further comprising:

determining that an error has occurred in the operation of at least one additional integrated circuit, wherein the additional integrated circuit is coupled to the non-volatile memory; and

saving the state of the at least one additional integrated circuit to the non-volatile memory when the error has been detected in the at least one additional integrated circuit.

23. The method of claim 20 wherein the state-saving controller is a separate component electrically coupled to the integrated circuit and to the non-volatile memory via a bus.

24. The method of claim 20 wherein the state-saving controller is integrated with and internal to the integrated circuit.

25. The method of claim 14 wherein the state of the integrated circuit is saved automatically upon the occurrence of the error, without receiving a request to save the state from a source outside the integrated circuit and state-saving controller.

26. The method of claim 14 wherein saving the state of the integrated circuit includes saving the data contents of registers and other latches of the integrated circuit.

27. A computer readable medium including program instructions to be implemented by a

computer, the program instructions implementing steps for saving the state of an integrated circuit, the steps comprising:

determining that an error has occurred in the operation of the integrated circuit; and

saving the state of the integrated circuit to a non-volatile memory coupled to the integrated circuit, the state saved after the error has been detected.

28. The computer readable medium of claim 27 wherein each latch of the integrated circuit is saved to the non-volatile memory.

29. The computer readable medium of claim 27 wherein the state is saved when the error is an unrecoverable error in the integrated circuit.

30. The computer readable medium of claim 27 wherein all internal clocks of the integrated circuit are stopped so that the latches retain their states upon the error in the operation of the integrated circuit.

31. The computer readable medium of claim 27 wherein an error flag is asserted after the state of the integrated circuit has been saved.

32. The computer readable medium of claim 31 wherein the error flag is provided to a service processor monitoring the operation of the integrated circuit.

33. The computer readable medium of claim 27 wherein the state of the integrated circuit is

saved by a state-saving controller coupled to the non-volatile memory and coupled to the integrated circuit.

34. The computer readable medium of claim 27, wherein the program instructions implement steps further comprising:

detecting an error in the operation of at least one additional integrated circuit, wherein the additional integrated circuit is coupled to the non-volatile memory; and

saving the state of the at least one additional integrated circuit to the non-volatile memory when the error has been detected in the at least one additional integrated circuit.

35. The computer readable medium of claim 33 wherein the state-saving controller is a separate component electrically coupled to the integrated circuit and to the non-volatile memory via a bus.

36. The computer readable medium of claim 33 wherein the state-saving controller is integrated with and internal to the integrated circuit.